



September 12, 2001

To: Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572  
20 McIntosh Drive  
Poughkeepsie, N.Y. 12603

#2  
Prior Art  
FJONES  
10-15-01

Subject:

Serial No. 09/898,386 07/05/01

Shui-Hung Chen, Jian-Hsing Lee,  
Jiaw-Ren Shih, Ta-Lee Yu

DIODE FOR POWER PROTECTION

Grp. Art Unit: 2811

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,002,568 to Ker et al., "ESD Protection  
Scheme for Mixed-Voltage CMOS Integrated Circuits," discloses  
an ESD circuit using silicon controlled rectifier (SCR)  
devices.

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U.S. Patent 5,898,205 to Lee, "Enhanced ESD Protection Circuitry," teaches an ESD protection circuit where conventional CMOS protection transistors are capacitively-coupled to improve performance.

U.S. Patent 6,011,681 to Ker et al., "Whole-Chip ESD Protection for CMOS ICS Using Bi-Directional SCRS," discloses a circuit using bi-directional SCR devices to provide current discharge paths between separate power supplies.

U.S. Patent 5,530,612 to Maloney, "Electrostatic Discharge Protection Circuits Using Biased and Terminated PNP Transistor Chains," teaches ESD protection circuits using biased diode strings and cantilevered diode strings.

U.S. Patent 5,747,834 to Chen et al., "Adjustable Bipolar SCR Holding Voltage for ESD Protection Circuits in High Speed Bipolar/BiCMOS Circuits," discloses a bipolar SCR with an adjustable holding voltage wherein the device is entirely constructed in an n-well and uses a buried layer.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', is written over the typed name.

Stephen B. Ackerman,  
Reg. No. 37761